Abstract of the Disclosure

A semiconductor memory device having sense amplifier array blocks between neighboring unit memory cell array blocks in a column direction, the semiconductor memory device includes a first sense amplifier driving line configured by passing the sense amplifiers in a row direction, a second sense amplifier driving line configured by passing the sense amplifiers in a row direction, a plurality of first NMOS transistors, which is disposed in the sense amplifier array block, for locally performing a pull-up operation of the first sense amplifier driving line in response to a first control signal, and a second NMOS transistor, which is disposed in a hole area, for performing a pull-down operation of the second sense amplifier driving line in response to a second control signal.